ABSTRACT OF THE DISCLOSURE

Circuitry for use with a general purpose performance counter ("GPPC") connected to a bus carrying a plurality of encoded state coverage signals indicative of test coverage in a logic design, wherein the circuitry is operable to decode and capture the encoded coverage information. A selection circuit associated with the GPPC is operable to select the encoded state coverage signals from a multi-bit event signal on the bus. A line decoder coupled to the selection circuit decodes the encoded state coverage signals into *N* one-hot signals, which are asserted based on coverage of corresponding states during test. A capture circuit is operable to capture the *N* one-hot signals for further processing.